APPARATUS AND METHOD FOR AMPLIFYING ANALOG SIGNAL AND ANALOG PREPROCESSING CIRCUITS AND IMAGE PICK-UP CIRCUITS

Related Application

This application relies for priority on Korean patent application number 03-51552, filed on July 25, 2003, the contents of which are incorporated herein in their entirety by reference.

Field of the Invention

The invention relates to image processing and, more particularly, to an analog front end (AFE) for a scanner, multi-function periphery (MFP), digital still camera (DSC) and/or a camcorder.

Background of the Invention

A conventional image processing system includes a charge-coupled device (CCD), an analog front end (AFE) and a digital image processor. The AFE interfaces between an analog device, e.g., CCD, and a digital device and functions to convert the analog data from the analog device to digital data for the digital device.

FIG. 1 is a conceptual block diagram illustrating an image processing system. An image of an object 110 is formed by an image forming element, depicted as a lens 120, onto an analog image detecting device such as a CCD 130. The AFE 140 converts the analog data from the CCD to digital data and forwards the converted digital data to a digital post processor 150, which processes the data to be transmitted to one or more data/display devices, such as computer 170-A, storage disk 170-B, printer/facsimile machine 170-C or camcorder 170-D.

The analog device used for acquiring the analog data for the image can be referred to as a sensor. The sensor can be a contact image sensor (CIS) in which the object is in contact with the system, such as a piece of paper on the glass of a copy machine, facsimile machine or scanner. The CIS can be a CCD CIS or a CMOS CIS.

FIG. 2 is a schematic block diagram of one example of an AFE 140 in an image processing system. The AFE 140 can be regarded as including two parts, namely, the

analog signal processing section and the digitizer. The analog signal processing section includes a correlated double sampler (CDS) 141 and a programmable gain amplifier (PGA) 142. The digitizer can include an analog-to-digital converter (ADC) 143. The CDS 141 receives the input analog image signal via an input terminal 144 and samples the input signal. The PGA 142 receives the sampled signals from the CDS 141, amplifies the samples using a variable gain and provides an output signal to the ADC 143. The ADC 143 digitizes the signal from the PGA 142 and provides the digital output at an output terminal 145.

FIG. 3 is a waveform diagram illustrating a typical input analog image signal. With reference to FIG. 3, for each pixel, the signal includes a reset portion, a black portion or reference portion and a signal portion as shown. The real signal or data portion of the signal extends between the dashed lines in the waveform diagram at points labeled 1 and 2.

At points 1 and 2, the CDS 141 samples the data signal. The CDS 141 subtracts the data signal from a reference signal, i.e., the black signal. The difference of the sampled data is a real signal.

With reference to FIG. 3, it is noted that the signal levels, and, in particular, the black reference signal, vary from pixel to pixel. This is due to different characteristics of the diodes in the pixels.

Summary of the Invention

In one aspect, the invention is directed to an image processing system and method. In accordance with the invention, an input receives an input signal. A correlated double sampler (CDS) receives the input signal, samples the input signal and provides an output signal. The CDS of the invention includes an amplifier for amplifying the input signal.

In one embodiment, gain in the CDS is settable to one of a plurality of levels. In one particular embodiment, the gain in the CDS is settable to one of four levels. In one embodiment, the four levels comprise 0.5, 1.0, 2.0 and 4.0.

The gain in the CDS can be settable to a level between 1.0 and 2.0.

The gain in the CDS is settable by a digital input signal. The digital input signal can contain a plurality of bits, and, in particular, can include two bits.

In one embodiment, the system includes a programmable gain amplifier (PGA) for receiving the output signal from the CDS and amplifying the received signal. The gain in the PGA can be settable to one of a plurality of levels. In particular, the gain in the PGA can be settable to one of four levels. The four levels can include 0.5, 1.0, 2.0 and 4.0.

The gain in the PGA can be settable to a level between 1.0 and 2.0.

In one embodiment, gain of the PGA is settable by a digital input signal. The digital input signal contains a plurality of bits. In one embodiment, a first portion of the bits is applied to the CDS to set the gain of the CDS and a second portion of the bits is applied to the PGA to set the gain in the PGA.

In one embodiment, an overall gain of the system comprises a combination of gain in the CDS and gain in the PGA. The overall gain can be pseudo-logarithmic.

In another aspect, the invention is directed to an image processing system and method. In accordance with the invention, a correlated double sampler (CDS) receives an input signal. The CDS samples the input signal and provides an output signal. The CDS includes an amplifier for amplifying the input signal. A programmable gain amplifier (PGA) receives the output signal from the CDS and amplifies the received signal.

In one embodiment, gain in the CDS is settable to one of a plurality of levels. In one particular embodiment, the gain in the CDS is settable to one of four levels. In one embodiment, the four levels comprise 0.5, 1.0, 2.0 and 4.0.

The gain in the CDS can be settable to a level between 1.0 and 2.0.

The gain in the PGA can be settable to one of a plurality of levels. In particular, the gain in the PGA can be settable to one of four levels. The four levels can include 0.5, 1.0, 2.0 and 4.0.

The gain in the PGA can be settable to a level between 1.0 and 2.0.

The gain in the CDS and the gain in the PGA are settable by a digital input signal. The digital input signal can contain a plurality of bits. In one embodiment, a first portion

of the bits is applied to the CDS to set the gain of the CDS and a second portion of the bits is applied to the PGA to set the gain in the PGA.

In one embodiment, an overall gain of the system comprises a combination of gain in the CDS and gain in the PGA. The overall gain can be pseudo-logarithmic.

Brief Description of the Drawings

The foregoing and other objects, features and advantages of the invention will be apparent from the more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

FIG. 1 contains a schematic block diagram of an image processing system.

FIG. 2 is a schematic block diagram of an analog front end (AFE) in an image processing system.

FIG. 3 is a waveform diagram illustrating a typical input analog image signal.

FIG. 4 is a schematic block diagram of a portion of the image processing system of the invention.

FIG. 5 is a schematic block diagram of an amplifier circuit using capacitors to set gain.

FIG. 6 is a schematic diagram illustrating amplification in an analog front end (AFE) in accordance with the present invention.

FIG. 7 is a schematic block diagram of one embodiment of an image processing system in accordance with the invention.

FIG. 8 is a schematic block diagram of one embodiment of a correlated double sampler (CDS) of the invention.

FIG. 9 is a schematic block diagram of one embodiment of a programmable gain amplifier (PGA) in accordance with the invention.

FIG. 10 is a table illustrating the gain in the CDS, the gain in the PGA and the overall DC gain for the gain setting values of the bits of the digital gain setting signal, in accordance with the invention.

FIG. 11 is a graph of the overall gain in the system of the invention.

FIG. 12 is a detailed schematic block diagram of a circuit for generating timing signals in the system of the invention.

FIG. 13 is a waveform diagram illustrating timing of signals in the circuits of the invention where clock signals do not overlap.

FIG. 14 is a waveform diagram illustrating timing of signals in the circuits of the invention where clock signals overlap.

Detailed Description of the Invention

As noted above, the PGA provides the output data amplified by a variable gain. Amplification can be achieved using operational amplifiers with switched capacitors. In such circuits, gain is achieved using the capacitor ratio. Where standard capacitor ratio is relied upon, either very large or very small capacitors are required to achieve a wide range of variable gain.

There are multiple gain methods which can be used in a PGA. In a linear scale method, the capacitors used are extremely large. As a result, the drive capability of the operational amplifiers must be large, resulting in an overall larger sized system. That is, to increase the drive capability, the size of the CDS needs to be large. The large size can slow the system's performance. In a log scale approach, small size and high speed can be realized. However, in such systems, the capacitor ratio is not a fixed number. This can make the circuit difficult to implement. In a pseudo log scale approach, the circuit can be simplified by using unit capacitors.

FIG. 4 is a schematic block diagram of a portion of the image processing system of the invention. Referring to FIG. 4, the system of the invention includes a CDS 210. The CDS 210 provides an output to a PGA 220, which provides an amplified output to the ADC 230. In accordance with the invention, both the PGA 220 and the CDS 210 have amplification gains. That is, the PGA 220 has a gain G2, and the CDS 210 has a gain G1. The gain G1 of the CDS 210 is controlled by a first input control signal, and the gain G2 of the PGA 220 is controlled by a second control signal. In one embodiment, as described in detail below, the system generates a digital input signal which is used to generate the two gain control signals. For example, the digital input signal can include a

plurality of bits. A first portion of the bits can be used to control the gain G1 of the CDS 210, and a second portion of the bits can be used to control the gain G2 of the PGA 220.

In the system of the invention in FIG. 4, the overall gain of the system is formed as the combination of two portions. That is, the overall gain of the system is a combination of the gain G1 of the CDS 210 and the gain G2 of the PGA 220. The input signal is first amplified by the CDS 210, and is then amplified by the PGA 220. This results in decreased chip size and decreased noise. Also, the combination of the gains G1 and G2 results in an overall gain that is a pseudo log scale gain, as described below in detail.

FIG. 5 is a schematic block diagram of an amplifier circuit using capacitors C1 and C2 to set gain. The amplifier circuit includes an operational amplifier 250 having first and second input terminals. A first capacitor C1 is connected between an input of the circuit and one of the input terminals of the operational amplifier 250. A second capacitor C2 is connected between the node at which C1 and the operational amplifier 250 are connected and the output of the operational amplifier 250. An input signal is applied at the input of the circuit at one of the terminals of the capacitor C1. The input signal is amplified according to a gain of the circuit. The amplified signal appears at the output of the operational amplifier 250.

The gain of the circuit is determined by the ratio of the capacitances of C1 and C2. That is, the gain G1 = C1/C2. For example, if the capacitance of C1 is 128C0 and the capacitance of C2 is 1C0, the gain of the circuit is 128, where C0 is a unit capacitance.

FIG. 6 is a schematic diagram illustrating amplification in an analog front end (AFE) in accordance with the present invention. The circuit of FIG. 6 includes amplification in the CDS and also amplification in the PGA. The gain of the CDS is referred to as G1, and the gain in the PGA is referred to as G2. The gains G1 and G2 are determined by capacitance ratios. Specifically, the gain G1 is determined by the ratio of capacitances C3 and C4, i.e., G1 = C3/C4. The gain G2 is determined by the ratio of capacitances C5 and C6, i.e., G2 = C5/C6. The overall or total gain G_T of the system is the product of gains G1 and G2, i.e., G_T = G1 X G2.

For example, if C3 = 4C0, C4 = 1C0, C5 = 32C0 and C6 = 1C0 , the gain G1 in the CDS is 4, and the gain G2 in the PGA is 32. The overall gain of the system is 128. The circuit area of the circuit of FIG. 6 is much less than that of the circuit of FIG. 5. That is, the circuit of FIG. 5 requires a higher total capacitance, i.e., 129C0 , than the circuit of FIG. 6, i.e., 38C0. If capacitance occupies a certain capacitance unit area, then the total area occupied by C1 and C2 in FIG. 5 can be said to be 129 unit areas. In contrast, the total capacitance in FIG. 6 occupies 38 unit areas.

FIG. 7 is a schematic block diagram of the system 200 in accordance with the invention. As shown in FIG. 7 and described above, the system 200 includes a CDS 210 and a PGA 220. Both the CDS 210 and the PGA 220 include amplifiers for providing gain. As shown in FIG. 7, both the CDS 210 and the PGA 220 receive portions of a multiple-bit digital input signal PGA for setting their respective gains. In the particular exemplary embodiment of FIG. 7, the overall gain is set by an eight-bit digital signal PGA[7:0]. In this particular embodiment, two bits PGA[7:6] are applied to the CDS 210 and are used to set the gain in the CDS 210. The remaining six bits PGA[5:0] are applied to the PGA 220 to set its gain. The CDS 210 receives the input analog signal Vin and a reference voltage Vref. The CDS 210 samples and amplifies the signal Vin according to the gain set by the signal bits PGA[7:6] to produce output signals Vcoutp and Vcoutn, which are applied to the PGA 220. The PGA amplifies the received signals from the CDS 210 according to the gain set by the signal bits PGA[5:0] to produce output signals Vpoutp and Vpoutn, which are applied as inputs to the ADC 243. The ADC 243 digitizes the received signals and generates a digitized output signal Vout.

Hence, in accordance with the invention, the input signal is processed and amplified in both the CDS and PGA stages. The gains in both stages are settable by the multiple-bit digital signal PGA[7:0]. A first portion of the bits is applied to set the gain in the CDS 210, and a second portion of the bits is applied to set the gain in the PGA 220.

FIG. 8 is a schematic block diagram of one embodiment of the correlated double sampler (CDS) 210 of the invention. Referring to FIG. 8, the CDS 210 receives as inputs the input data signal Vin, a reference signal Vref_in, a reference signal Vref_b and a signal Vdac_in. The signal Vref_in provides the black level voltage for the input signal. The difference between Vref_in and Vin is the real video signal. The difference between

the signals Vdac_in and Vref_b is an offset voltage Voffset. Sampling transistors T1 through T4 sample the input signals under the control of sampling control clock signals QC1 and QC2. The sampled inputs are applied to the input side a variable capacitance unit 251, which includes two variable input capacitances Ci1 and Ci2. The values of the capacitances Ci1 and Ci2 are set according to the states of the two control input signal bits PGA[7:6].

Feedback capacitors Cf1 and Cf2 are connected to the inverting and noninverting inputs, respectively, of the operational amplifier 249. Transistors T7 and T8 selectively connect and bypass the feedback capacitor Cf1 under the control of control signals QC2 and QC1P. Transistors T9 and T10 selectively connect and bypass the feedback capacitor Cf2 under the control of control signals QC2 and QC1P. The signal Vrefm is selectively applied to the feedback capacitors Cf1 and Cf2 under the control of transistors T5 and T6 and timing signals QC1.

The CDS samples and amplifies the input signal to provide an output signal Vout. The output signal Vout is the difference between the output signals from the operational amplifier, that is, Vout = Vcoutp – Vcoutn.

The gain of the amplifier circuit in the CDS of FIG. 8 is set by the ratio of the capacitances. Under charge conservation, the following equation results:

$$Vout = Ci/Cf\,(Vref\_in - Vin + Voffset) - Vref$$

The CDS of the invention therefore includes a programmable gain amplifier. The gain of the CDS is Ci/Cf, since Ci1 = Ci2 = Ci, and Cf1 = Cf2 = Cf. The input capacitors Ci are settable via the input signals bits PGA[7:6]. With the two input bits, both of the capacitors are settable to one of four possible levels. As shown in FIG. 8, if the feedback capacitances are each C, then, in one particular embodiment, the input capacitors are settable to, for example, .5C, 1C, 2C and 4C. Accordingly, the gain of the CDS is settable to one of four values, namely, .5, 1.0, 2.0 and 4.0. The sampled and amplified output signal is applied to the programmable gain amplifier PGA 220.

FIG. 9 is a schematic block diagram of one embodiment of a PGA 220 in accordance with the invention. The PGA 220 includes a first plurality of 128 switched capacitors Cp0 through Cp127. These capacitors are selectively connected to the inverting input of the operational amplifier 349 under the control of the first switch

control 351 and a plurality of connected switches. Under the control of the remaining digital signal bits PGA[5:0], the switch control 351 determines for each capacitor Cp0 through Cp127 whether the capacitor is connected to the CDS output signal Vcoutp, the reference voltage Vrefm or the output signal Vpoutp of the operational amplifier 349. The switch control 351 also receives the control signals QC2 and QC2B and uses them in selecting the connections of the capacitors. The PGA 220 also includes a second plurality of 128 switched capacitors Cn0 through Cn127. These capacitors are selectively connected to the noninverting input of the operational amplifier 349 under the control of the second switch control 353 and a plurality of connected switches. Under the control of the remaining digital signal bits PGA[5:0], the switch control 353 determines for each capacitor Cn0 through Cn127 whether the capacitor is connected to the CDS output signal Vcoutn, the reference voltage Vrefm or the output signal Vpoutn of the operational amplifier 349. The switch control 353 also receives the control signals QC2 and QC2B and uses them in selecting the connections of the capacitors.

Transistors T11 and T12 selectively connect and bypass the feedback capacitance under the control of the signal QC2P.

The PGA circuit of FIG. 9 operates in an input mode and an output mode.

Under charge conservation, the following results for the circuit of FIG. 9.

$$(128 - y)C \times (Vpoutp - Vpoutn) = 128C \times (Vcoutp - Vcoutn)$$

$$Vpoutp - Vpoutn = 128C/(128 - y)C \times (Vcoutp - Vcoutn)$$

$$Vout = (2^{(6+1)}) / (2^{(6+1)} - y) \times Vin = (128 / 128 - y) \times Vin$$

In the above, Cp = Cn = C; y is an integer between from 1 to 64.

The gain in the PGA of FIG. 9 is given by (128) / (128 – y). Therefore, with y in the range from 1 to 64, the gain of the PGA is in the range from approximately 1 to 2.

Operation of the switch controls 351 and 353 is in accordance with the following. When QC2 is logic high, QC2B is logic low. The bits PGA[5:0] are don't care states, that is, their states are irrelevant. In this state, all upper switches are controlled by the switch control 351, 353 to be connected to Vcoutp, and all lower switches are controlled to be connected to Vcoutn. As a result, the numerator in the gain expression above is 128.

When QC2B is in a high logic state, QC2 is in a low logic state. The PGA[5:0] gain setting bits determine which of the switches are connected to Vrefm and which are

connected to Vpoutp. This is determined by the desired gain of the PGA. For example, if the bits PGA[5:0} are 000000, one switch is connected to Vrefm and 127 switches are connected to Vpoutp. If the bits PGA[5:0] are 111111, 64 switches are connected to Vrefm and 64 switches are connected to Vpoutp. This control scheme allows the parameter y in the denominator of the gain expression above to vary from 1 to 64, thus allowing the gain of the PGA to vary from 128/127 (1.008) to 2. FIG. 10 is a table illustrating the gain in the CDS (labeled A), the gain in the PGA (labeled B), the overall DC gain (V/V) and the overall DC gain (dB) for the gain setting values of the bits of the digital gain setting signal, i.e., PGA[7:6] and PGA[5:0]. FIG. 11 is a graph of the overall gain. In the graph, the control step is the value of the bits PGA[7:0], ranging from 0 to 255. With reference to FIG. 11, it is noted that the gain of the system of the invention is an almost perfect log scale, i.e., it is a pseudo log scale.

FIG. 12 is a detailed schematic block diagram of a circuit for generating timing signals in the system of the invention. In the circuit of FIG. 12, two clock signals CLK1 and CLK2 are used to generate the timing signals described and illustrated herein. In general, the signal CLK1 is conventionally used to sample the input video signal in the black level interval (see FIG. 3). The signal CLK2 is used to control sampling of the video signal during the video data portion of the signal. However, with reference to FIG. 14, it is possible that the signals CLK1 and CLK2 overlap in time, causing distortion of the samples of the input signal. FIG. 14 is a waveform diagram illustrating timing of signals in the circuits of the invention where clock signals overlap. FIG. 13 is a waveform diagram illustrating timing of signals in the circuits of the invention where clock signals do not overlap.

In order to avoid the condition of overlapping clock signals, the present invention uses signals other than the signals CLK1 and CLK2 to sample the input signal. Specifically, as described above and as shown in the drawings, the system of the invention uses the signals QC1 and QC2 to control the sampling. These signals are derived from the clock signals CLK1 and CLK2 as shown in the circuit diagram of FIG. 12.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that

various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

For example, throughout the foregoing description, the CDS is described has receiving two control bits to control the capacitance of input capacitors to set a gain to one of four levels. The PGA is described as having switch controls and switched capacitors. It should be noted that these amplification approaches may be reversed. That is, the CDS may use the switched capacitor approach instead of the PGA.